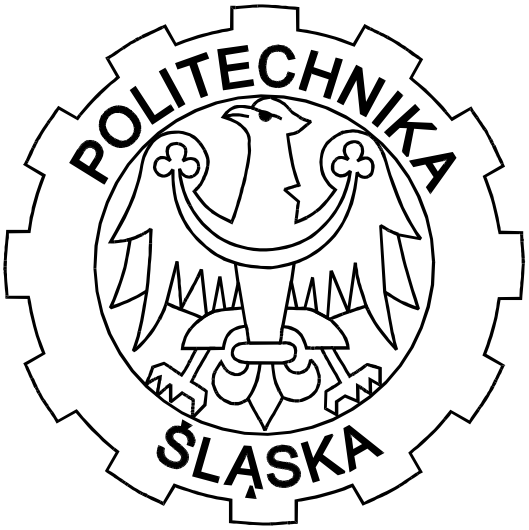

POLITECHNIKA ŚLĄSKA W GLIWICACH
WYDZIAŁ ELEKTRYCZNY

Katedra Energoelektroniki, Napędu Elektrycznego i Robotyki

ROZPRAWA DOKTORSKA

mgr inż. Krzysztof Przybyła

Analiza i badania wysokoczęstotliwościowych falowników klasy DE z tranzystorami MOSFET na bazie SiC i GaN

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Gliwice 2019

The possibility of application of SiC/GaN MOSFET transistors in a class DE inverter of 13.56 MHz band is evaluated in the dissertation. The author has not found any publications in polish language concerning resonant class DE and E inverters of 13.56 MHz band, build with SiC/GaN MOSFET transistors. Research about high frequency inverters built with dedicated silicon MOSFET transistors from IXYS was done in the Department of Power Electronics, Electrical Drives and Robotics of the Silesian University of Technology. Total efficiency of the measured inverters was $\eta_I \leq 80\%$. The causes of relatively low efficiency were large idle losses of applied dedicated integrated drivers from IXYS and high $R_{DS(on)}$ value of dedicated Si MOSFET transistors from IXYS (DE375-102N10A, 1000V/10A).

Four versions of class DE inverters with SiC/GaN MOSFET transistors were built and measured. Total efficiency of $\eta_I \approx 90\%$ was achieved in a continuous operation mode with the inverters built with GaN MOSFET transistors. The inverters with SiC MOSFET transistors had maximal total efficiency of $\eta_I \approx 80\%$ in a continuous operation mode. The dominant power losses are switching losses, estimated by 60%.

The result of conducted research is also the proposed C_{DRI} parameter, which characterizes integrated driver idle losses. At the moment in literature and datasheets of transistors there are no parameters that allow calculation and comparison of integrated driver idle power losses.

The computer model of a Class DE inverter was elaborated, that includes:

- Effective drain resistance R_{DSeffT}, that takes into account increase of resistance with temperature and frequency,
- Effective output resistance $R_{OSSeffT}$, that takes into account power losses in a transistor output capacitance,
- Transistor model with linear decline of drain current,
- Parasitic resistance of a matching network, that takes into account increase of air coil resistance with temperature and frequency,

The proposed model of a class DE inverter gives results, that are consistent with the measurement results by 10 percentage points.